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APPLICATION FOR LETTERS PATENT

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TECHNIQUE FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE WITHOUT CORNER EXPOSURE AND RESULTING STRUCTURE

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TITLE OF THE INVENTION

TECHNIQUE FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE WITHOUT CORNER EXPOSURE AND RESULTING STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of application Serial No. 08/789,470, filed January 27, 1997, pending.

BACKGROUND OF THE INVENTION

[0001] Field of the Invention: The present invention relates to an apparatus and method for forming a shallow trench isolation structure. More particularly, the present invention relates to forming the shallow trench isolation structure using a buffer film layer etched such that a capped trench structure is formed which isolates the shallow trench corners.

[0002] State of the Art: The semiconductor industry continually strives to increase semiconductor device performance and density by miniaturizing the individual semiconductor components and by miniaturizing the overall semiconductor device dimensions. For example, the semiconductor device density can be increased by more densely integrating the components on the semiconductor chip. However, increasing integration densities by placing the individual circuit elements in closer proximity increases the potential for interactions between the circuit elements. Therefore, it has become necessary to include isolation structures to prevent any significant interaction between circuit elements on the same chip.

[0003] Contemporary CMOS technologies generally employ field effect transistors that are adjacent or bounded by trenches. These trenches provide isolation (shallow trench isolation or "STI") for the semiconductor devices. However, the close proximity of each semiconductor device to an edge or corner of the trench may create parasitic leakage paths. The parasitic leakage paths result from an enhancement of the gate electric field near the trench corners. This gate electric field is enhanced by the trench corner's small radius of curvature and the proximity of the gate conductor. As a result of the enhanced gate electric field, the trench corner has a lower threshold voltage (V_t) than the planar portion of the device.

[0004] Presently known formation techniques for such trenches generally involve a wet etch, which can exacerbate the parasitic leakage problem by sharpening the trench corners and thinning the gate dielectric near the trench corner. Furthermore, present trench formation techniques generally expose the trench corners before gate electrode deposition. The exposure of trench corners will increase the sub-V_t leakage and degrade gate oxide integrity. The aforementioned problems will be hereinafter referred to collectively as "corner effects."

[0005] Corner effects can even dominate on-currents in applications such as DRAM chips that require narrow channel widths to achieve high density. This parallel current-carrying corner effect becomes the dominant MOSFET contributor to standby current in low standby power logic applications and to leakage in DRAM cells. Furthermore, there exists concern that the enhanced electric fields due to field crowding at the trench corner may impact dielectric integrity.

[0006] Numerous techniques have been proposed to overcome the above discussed corner effects. Commonly-owned U.S. Patent 5,433,794, issued July 18, 1995 to Fazan et al., hereby incorporated herein by reference, and U.S. Patent 5,521,422, issued May 28, 1996 to Mandelman et al., each teach forming shallow trench isolation structures wherein insulating material spacers are formed abutting the trench corners and the isolating material filling and extending above the trench. When a wet pad oxide etch is performed, the isolating material combines with the spacers to form an isolation trench having a dome or cap-like covering the peripheral edges of the trench which substantially overcomes the corner effects and consequential leakage between active areas on the substrate. Although the techniques taught in these patents are effective in minimizing corner effects, the techniques require additional fabrication steps which increase the overall cost of the semiconductor component.

[0007] U.S. Patent 5,436,488, issued July 25, 1995 to Poon et al., teaches improving trench isolation by increasing the thickness of the gate dielectric overlying the trench corner between the substrate and gate electrode. However, the process taught in this patent also requires numerous additional fabrication steps and structures, which of course increase the overall cost of the semiconductor component.

[0008] Therefore, it would be advantageous to develop a shallow isolation trench and a technique for forming the trench which substantially eliminates the aforementioned corner effects, while using inexpensive, commercially-available, widely-practiced semiconductor device fabrication techniques and apparatus.

SUMMARY OF THE INVENTION

[0009] The present invention relates to a shallow isolation trench structure which is formed using a buffer film layer. The buffer film layer is etched in such a manner that an isolation material within the shallow trench has a cap which covers the shallow trench corners to prevent corner effects.

[0010] The method of the present invention comprises providing a semiconductor substrate, preferably a silicon substrate, with a dielectric layer, preferably silicon dioxide, formed on at least one surface of the semiconductor substrate to a thickness of between 50 and 300Å. The dielectric layer can be formed by any known technique, including thermally oxidizing the surface of the semiconductor substrate, chemical vapor deposition, sputtering, or the like. A buffer film layer, preferably silicon nitride, is then formed over the dielectric layer by any known deposition technique, preferably chemical vapor deposition. Although silicon nitride is preferred, the buffer layer may be any known material which is oxidation resistant and can be etched selectively to oxide films.

[0011] A photoresist mask is applied and patterned on the buffer film layer. The buffer film layer, the dielectric layer, and semiconductor substrate are then etched either simultaneously with a non-selective etch or in steps with selective etches to form a shallow trench with sidewalls and a bottom. The photoresist mask is then removed to form a trenched structure.

[0012] After stripping the photoresist and cleaning the trenched structure, a thin layer of oxide, between about 50 and 150Å thick, is grown on the shallow trench sidewalls and bottom, preferably by thermal oxidization. The buffer film layer is then selectively etched horizontally and vertically to move the buffer film layer back from the shallow trench. The purpose for using a buffer film layer, which is oxidation resistant, as discussed above, is shown in FIG. 11. If an oxidizable material is used as a buffer film layer 202 over a dielectric layer 204 and a substrate

206, the formation of a thin oxide layer 208 in trench 210 would also cause the formation of an additional thin layer of oxide 212 to form on the buffer film layer 202. Most oxidizable materials, such as silicon dioxide, used for forming the buffer film layer 202 have a greater affinity for growing oxides than the semiconductor substrate. As a result, the additional thin oxide layer 212 is relatively thicker than the thin oxide layer 208, which results in a narrowing of the opening at the mouth of the trench 210. This narrowing makes it difficult to fill the trench 210 with an isolation material 214, and may even cause the formation of voids 216 in the isolation material 214 during the application of the isolation material 214.

[0013] In the method of the present invention, after etching back the buffer film layer, the shallow trench is then filled with an isolation material. The resulting structure is preferably annealed to densify the deposited isolation material. Densification of the deposited isolation material is required to enhance the resistance of the isolation material to etching during subsequent processing. A portion of the isolation material over the buffer film layer is then removed to the level of the buffer film layer. The removal of isolation material is preferably achieved with a process such as chemical mechanical planarization which abrades away the isolation material down to the buffer film layer. The buffer film layer is then selectively etched away to form an isolation structure. When this isolation structure is etched during a subsequent wet oxide etch process, the isolation structure will form the capped shallow trench isolation structure which covers the trench corners. This capped shallow trench isolation structure substantially minimizes corner effects.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

[0015] FIGS. 1-10 are cross-sectional views of the method of forming a shallow trench isolation structure of the present invention; and

[0016] FIG. 11 is a cross-sectional view of a shallow trench isolation structure formed with a conventional oxidizable buffer film layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] FIGS. 1 through 10 illustrate, in cross-section, a method for forming a shallow trench isolation structure in accordance with one embodiment of the present invention. As shown in FIG. 1, the method comprises forming a layered structure 100 of a semiconductor substrate 102, a dielectric layer 104, and a buffer film layer 106. The semiconductor substrate 102 preferably includes silicon and the dielectric layer 104 preferably includes silicon dioxide. The dielectric layer 104 is preferably between 50 and 300Å thick (a convenient range for process integration) and can be formed by any known technique including thermally oxidizing the surface of the semiconductor substrate 102, chemical vapor deposition, sputtering, or the like. The buffer film layer 106, preferably comprising silicon nitride, is formed over the dielectric layer 104 by any known deposition technique, preferably chemical vapor deposition.

[0018] A photoresist mask 108, either a positive or negative resist (preferably positive) as known in the art, is applied over the buffer film layer 106 and patterned using standard photolithographic patterning techniques, as shown in FIG. 2. The buffer film layer 106 and the dielectric layer 104 are then etched by standard etching techniques to form patterned recess 110, as shown in FIG. 3. The silicon substrate 102 is then dry etched to form a shallow trench 112 with sidewalls 114 and a bottom 116, seen in FIG. 4. It is, of course, understood that the buffer film layer 106, the dielectric layer 104, and semiconductor substrate 102 can be etched in one non-selective etching step. The photoresist mask 108 is removed using standard photoresist stripping techniques, preferably by plasma etch, to form a trenched structure 118, as shown in FIG. 4.

[0019] After stripping the photoresist and cleaning (preferably with an H_2O_2/H_2SO_4 or H_2O_2/HCl mixture) the trenched structure 118, a thin layer of oxide 120, between about 50 and 150Å thick, is grown on the shallow trench sidewalls 114 and the shallow trench bottom 116, preferably by thermal oxidization, as shown in FIG. 5. As shown in FIG. 6, the buffer film layer 106 is then selectively etched horizontally and vertically to move the buffer film layer 106

back from the shallow trench 112. The etching of the buffer film layer 106 is preferably a wet etch process including an application of a 100:1 HF (hydrofluoric acid) solution followed by an application of a H_3PO_4 (phosphoric acid) solution or an $H2O/N(CH_2CH_3)_4OH$ ("TMAH") solution.

[0020] The shallow trench 112 is then filled with an isolation material 122, as shown in FIG. 7. The isolation material 122 is preferably silicon dioxide deposited by any known technique including chemical vapor deposition using tetraethylorthosilane (TEOS) or ozone as source gases, electron cyclotron resonance deposition, spin-on deposition, and the like. Optionally, the isolation material 122 can be annealed to densify the deposited isolation material 122. Densification of the deposited isolation material 122 is used to enhance the resistance of the isolation material 122 to etching during subsequent processing. The annealing is preferably conducted in a nitrogen or other inert gas atmosphere to prevent oxidation of the semiconductor substrate 102 beneath the isolation material 122.

[0021] As shown in FIG. 8, the isolation material 122 is removed down to the buffer film layer 106, preferably by a mechanical abrasion process, such as chemical/mechanical planarization. The buffer film layer 106 is then selectively etched away, by any known technique such as a hot H_3PO_4 (phosphoric acid), to form an isolation structure 124, as shown in FIG. 9. When this isolation structure 124 is etched during a subsequent wet oxide process to expose the upper surface 132 of said semiconductor substrate 102, the isolation structure 124 will form a capped shallow trench isolation structure 126 which covers the trench corners 128 of the shallow trench 112 with ledges 130, as shown in FIG. 10. The ledges 130 preferably extend horizontally between about 50 and 150Å from the trench corners 128. These ledges 130 prevent the aforementioned corner effects.

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[0022] Having thus described in detail preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by

particular details set forth in the above description, as many apparent variations are possible without departing from the spirit or scope thereof.